SD8108X
20 bits ADC SoC with LED Drive

Features

- High precision ADC, 17.4bits ENOB at 8sps and 200x Gain, 1 differential or 3 single-ended inputs, with offset calibration capability
- Low noise, high input impedance preamplifier with selectable gain: 1, 12.5, 50, 100, or 200
- 8 bits RISC ultra low power MCU, 49 instructions and 6 stack levels. The MCU current consumption is 600uA typically at 3V and 2MHz operating clock rate, 2uA at standby and 32kHz clock, and 1uA at sleep
- 16k Bytes OTP, 256 Bytes SRAM
- Built-in OTP with low programming voltage at 2.4V~3.6V, can replace external EEPROM
- Internal RC oscillator. No external clock source needed
- 8 bits interrupt timer
- Built-in temperature sensor, supports single point calibration
- 8 LED ports that can drive up to 56 LEDs, 72mA sink current, source current selectable at 4.5/6/7.5/9/10.5/12mA, LED duty cycle selectable
- Selectable voltage source for external transducer excitation: 2.4V/2.6V/2.9V/3.3V
- Flexible battery voltage detection: 2.0V~3.3V
- Schmitt trigger input, pull up resistor selectable
- Watch Dog Timer
- Low voltage detection and power on reset circuit
- Operating voltage range: 2.4V~3.6V
- Operating temperature range: -40˚C~85˚C

Description

The SD8108X is a CMOS SoC with built-in 20 bits ADC and 16k Bytes OTP memory. Very few external components are needed to implement body weight scale or kitchen scale with LED displays.

The IC was designed with ultra low power technology. Operating at 3V supply and 2MHz clock rate that originates from 4MHz internal RC oscillator, the total typical operating current is 850uA (external transducer driving and LED currents not included).

Three working modes are provided so users can select the optimum choice between speed and power. They are normal mode, standby mode, and sleep mode.

Applications

Body weight scale, kitchen scale, palm scale, portable scale, tire pressure scale

Ordering Information

SOP16

Pin Diagram and Descriptions

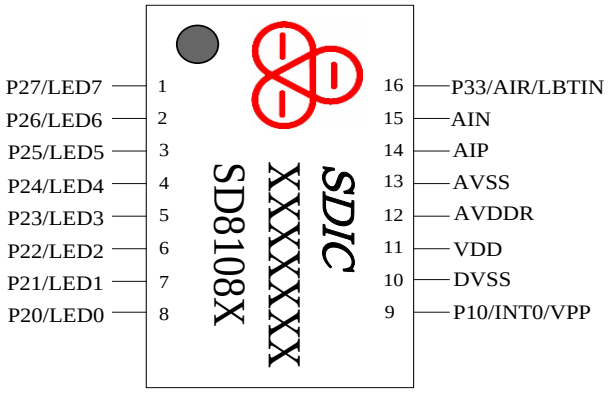


Figure 1. SOP16 pin out diagram

Table 1. Pin Descriptions

Pin No.	Pin Name	Attribute	Description
1	P27/LED7	I/O	Digital port P27 or LED7 driver
2	P26/LED6	I/O	Digital port P26 or LED6 driver
3	P25/LED5	I/O	Digital port P25 or LED5 driver
4	P24/LED4	I/O	Digital port P24 or LED4 driver
5	P23/LED3	I/O	Digital port P23 or LED3 driver
6	P22/LED2	I/O	Digital port P22 or LED2 driver
7	P21/LED1	I/O	Digital port P21 or LED1 driver
8	P20/LED0	I/O	Digital port P20 or LED0 driver
9	P10/INT0/VPP	Analog, I	Digital input port P10 or external interrupt INT0, also used as OTP high voltage programming pin, connect 1uF capacitor to DVSS
10	DVSS	Ground	Digital ground
11	VDD	Power	Power supply voltage, connect 1uF capacitor to DVSS, the capacitor should be very close to the IC
12	AVDDR	Analog	External transducer power source, connect 0.1uF filter capacitor to AVSS
13	AVSS	Ground	Analog ground
14	AIP	Analog input	Analog signal differential inputs Should enable the internal pull-down resistor when not used
15	AIN		
16	P33/AIR/LBTIN	Analog, I/O	Digital port P33, AIR (with AVSS) as ADC analog input or reference voltage input, or external voltage level detect LBTIN input

Remark: All I/O ports Pnn have internal pull-up option (default OFF) and input hysteresis at 0.3VDD/0.7VDD.

Functional Block

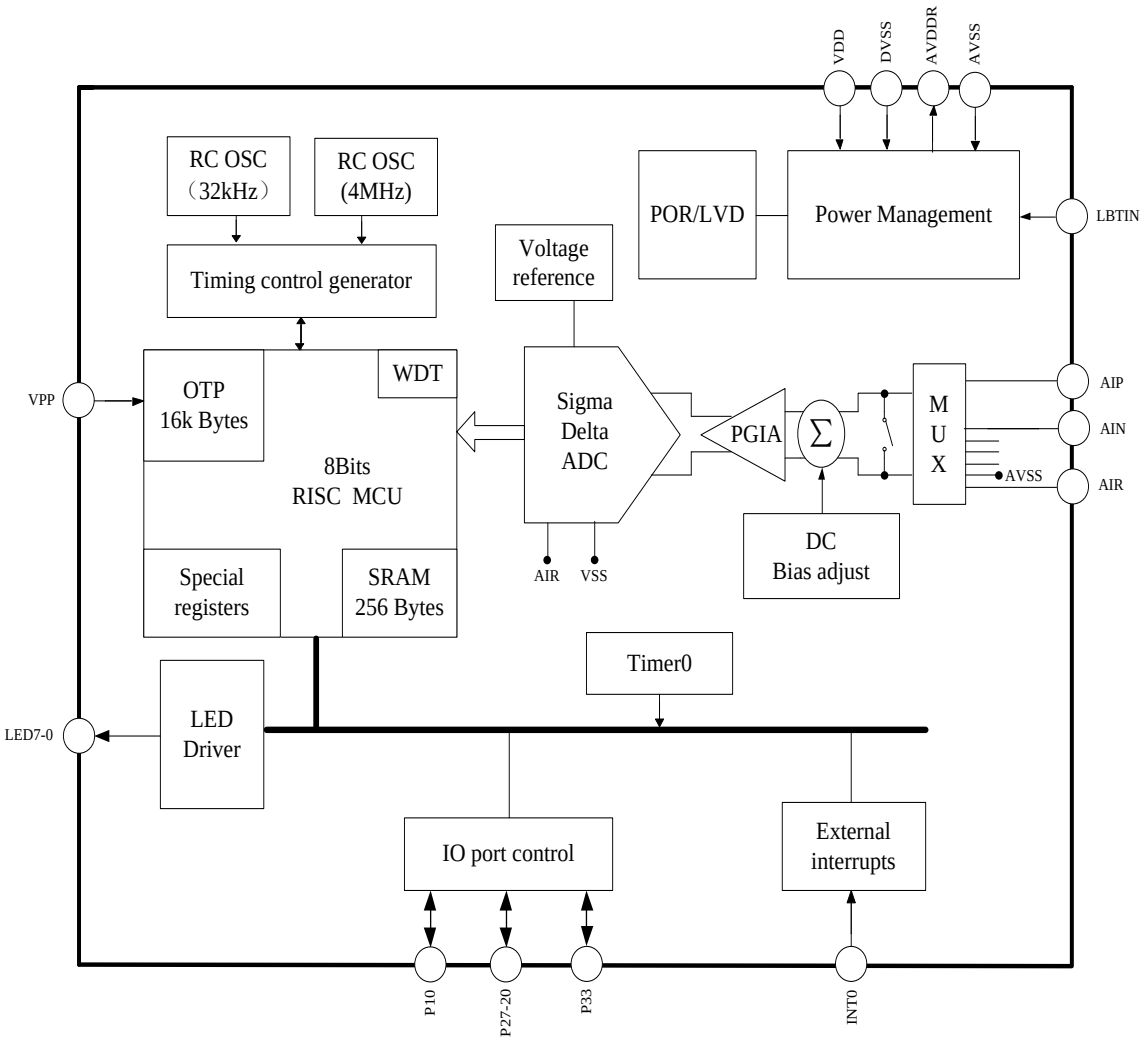
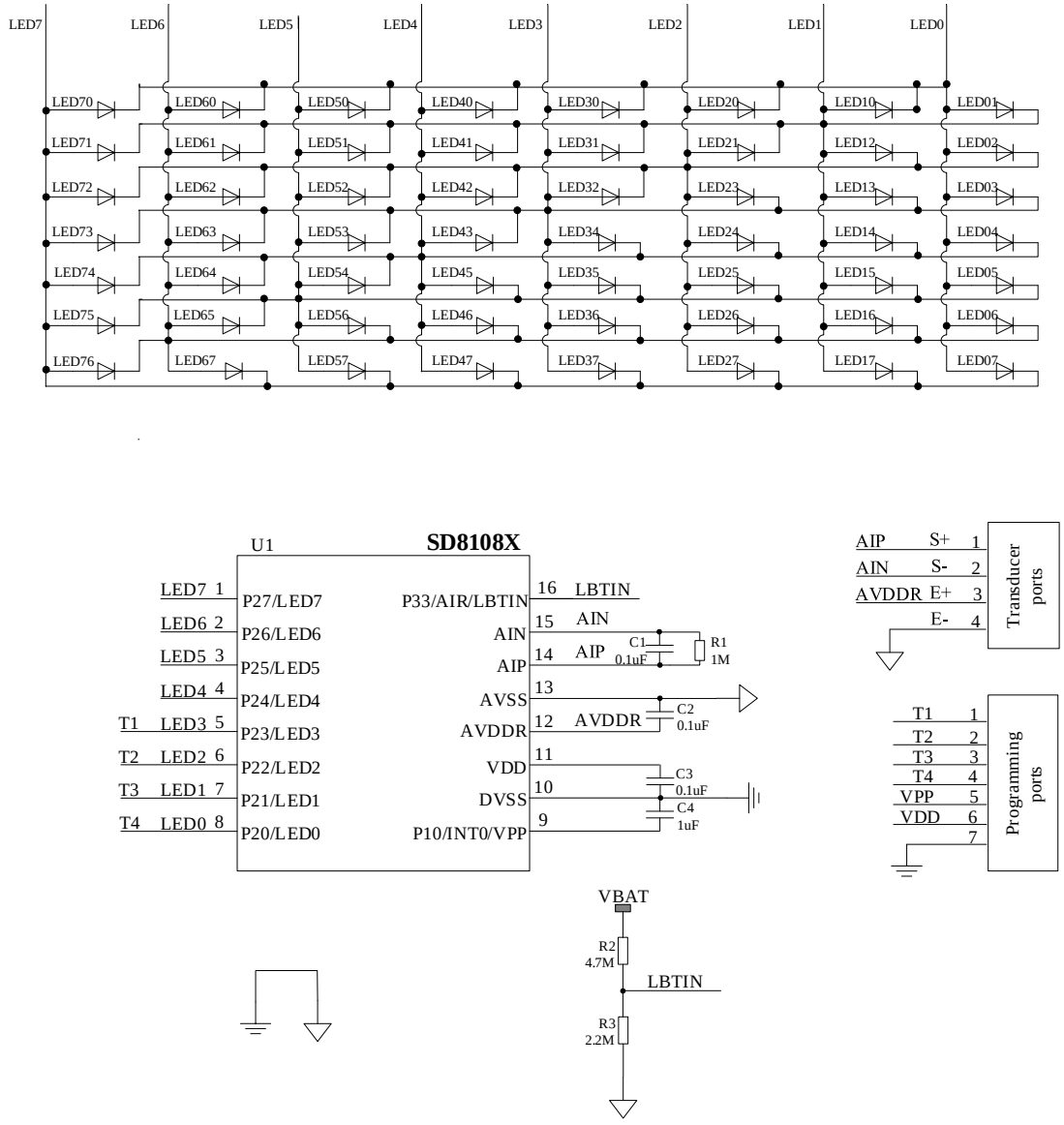


Figure 2. Functional block diagram

Typical Applications



1. Power and LED ports lines should be as wide as possible.
2. Use bigger capacitor between VDD/DVSS as VDD drives increases.
   It should be very close to the IC.

Figure 3. Typical application diagram

ADC Characteristics

Table 2. ENOB and voltage noise Vn_{rms} (AVDDR=2.4V, VREF=0.6V, SINC3, Buffer on)

ADC sampling rate = 128kHz										
OSR			128	256	512	1024	2048	4096	8192	16384
Gain	**200**	**ENOB**	13.8	14.4	15.0	15.3	16.0	16.4	16.9	17.4
		Vn_{rms}(nV)	376.6	278.4	190.8	141.8	94.4	66.7	48.4	35.1
	100	**ENOB**	14.8	15.4	15.8	16.4	16.9	17.5	17.9	18.3
		Vn_{rms}(nV)	393.3	288.5	213.0	141.6	99.5	66.7	50.2	36.9
	1	**ENOB**	16.4	17.0	17.4	17.8	18.2	18.7	19.1	19.9
		Vn_{rms}(nV)	13735.2	8885.7	6552.7	4757.7	3548.3	2728.5	1711.6	1141.3

ADC sampling rate = 256kHz										
OSR			128	256	512	1024	2048	4096	8192	16384
Gain	**200**	**ENOB**	13.8	14.0	14.7	15.0	15.6	16.2	16.6	17.1
		Vn_{rms}(nV)	439.0	315.2	221.4	170.0	122.6	81.9	59.0	40.7
	100	**ENOB**	14.5	15.1	15.7	16.1	16.6	17.1	17.6	18.1
		Vn_{rms}(nV)	487.3	449.3	235.4	166.4	124.8	85.1	59.7	42.3
	1	**ENOB**	16.4	16.9	17.3	17.7	18.1	18.6	19.1	19.7
		Vn_{rms}(nV)	15202.4	10074.8	7143.6	5407.7	4118.2	3077.6	2168.3	1408.1

Remark:

The above data are averages based on multiple ICs' measured results. Each IC contributes 1024 data points.

ENOB = $\log_2\left(\frac{FSR}{Vn_{rms}}\right)$, FSR is the Full Scale Voltage Range (2 * Vref / Gain), Vrms is the rms Noise.

Oscillator Characteristics

Figure 4 and figure 5 are SD8108X oscillating frequency as function of power supply voltage from five parts.

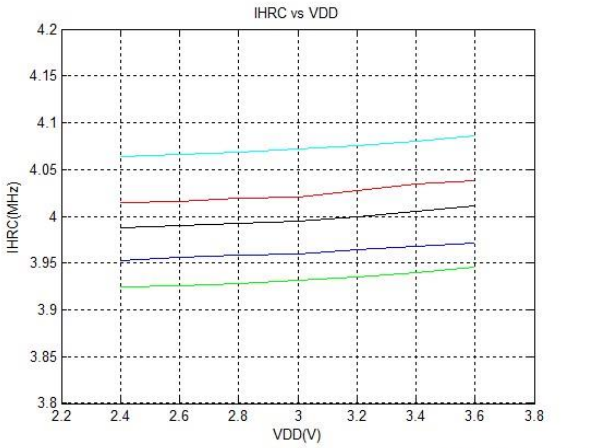


Figure 4. IHRC frequency vs voltage

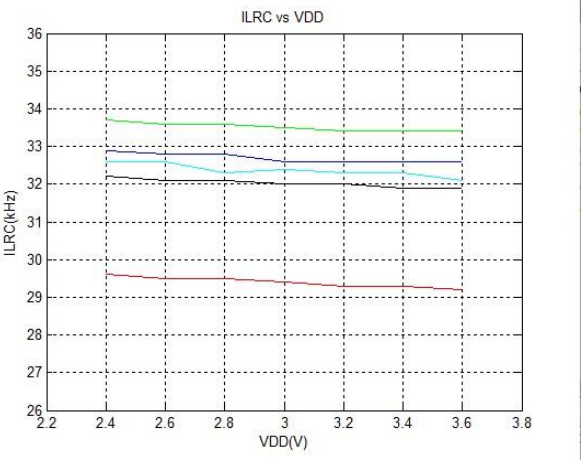


Figure 5. ILRC frequency vs voltage

Figure 6 and figure 7 are SD8108X oscillating frequency as function of temperature from five parts.

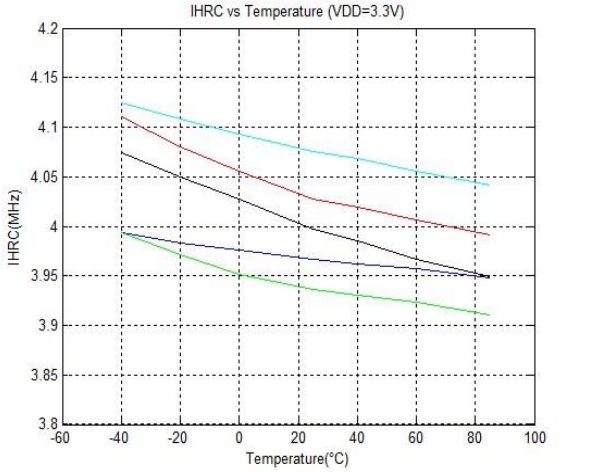


Figure 6. IHRC frequency vs temperature

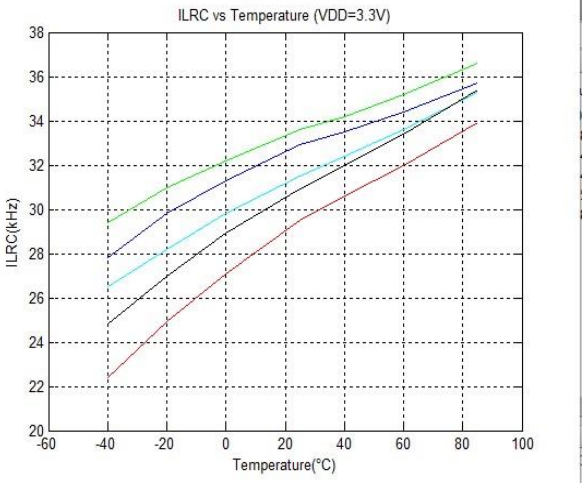


Figure 7. ILRC frequency vs temperature

Electrical Specification

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
T_A	Operating temperature	-40	+85	℃
T_S	Storage temperature	-55	+150	℃
V_{DD}	Supply voltage	-0.2	+4.0	V
Vpp	Programming voltage	-0.2	+6.75	V
V_{IN}, V_{OUT}	Digital input/output voltage	-0.2	V_{DD}+0.3	V
T_L	Reflow temperature profile	Per IPC/JEDECJ-STD-020C		℃

Remarks:

1. CMOS device can easily be damaged by electrostatics. It must be stored in conductive foam, and careful not to exceed the operating voltage range.
2. Turn off power before insert or remove the device.

Table 4. Electrical Specifications (VDD=3V, T_A=25 ˚C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Remarks
VDD	Supply voltage	2.4	3.0	3.6	V	Analog modules operating voltage
		2.0	3.0	3.6	V	Digital modules and MCU operating voltage
FOSC	Operating frequency	0.016	2	4	MHz	FOSC must be 2MHz when read/write tables in OTP
IHRC	Internal high frequency RC oscillator	--	4	--	MHz	Frequency after calibration
ILRC	Internal low frequency RC oscillator	--	32	--	kHz	Frequency after calibration
IDD1	Operating current 1	--	850	--	uA	4MHz internal RC oscillator freq halved for MCU Digital and analog modules both active
IDD2	Operating current 2	--	2	--	uA	32kHz internal RC oscillator for MCU MCU at standby mode Analog modules inactive
IDD3	Operating current 3	--	1	--	uA	MCU at sleep mode Analog modules inactive
Fsam	ADC sampling rate	--	--	256	kHz	
OSR	Over sampling rate	128	--	16384		
NFbit	Noise free bits[1]	--	16	--	bits	Gain=200, input FSR=±4mV
VINpga	PGIA differential input range[2]	-Vref[3]	--	Vref	mV	1X gain
		-Vref/12.5	--	Vref/12.5		12.5X gain
		-Vref/50	--	Vref/50		50X gain
		-Vref/100	--	Vref/100		100 X gain
		-Vref/200	--	Vref/200		200 X gain

Vavddr	AVDDR Voltage output	--	2.4	--	V	AVDDRX [1:0]=00
		--	2.6	--		AVDDRX [1:0]=01
		--	2.9	--		AVDDRX [1:0]=10
		--	3.3	--		AVDDRX [1:0]=11
Iavddr	AVDDR current	--	10	--	mA	--
POR	POR voltage	--	1.5	--	V	--
LVD	LVD voltage	--	1.9	--	V	--
THlbt	LVD hysteresis	--	100	--	mV	--
Vlbt	Low VDD alarm threshold	--	--	--	V	LBTX[3:0]=0000: Vlbt OFF
		--	LBTIN	--		LBTX[3:0]=1000
		--	3.3	--		LBTX[3:0]=0001
		--	3.2	--		LBTX[3:0]=0010
		--	3.1	--		LBTX[3:0]=0011
		--	3.0			LBTX[3:0]=1001
		--	2.9	--		LBTX[3:0]=1010
		--	2.8	--		LBTX[3:0]=1011
		--	2.7	--		LBTX[3:0]=1100
		--	2.6	--		LBTX[3:0]=1101
		--	2.5	--		LBTX[3:0]=1110
		--	2.4	--		LBTX[3:0]=1111
		--	2.3	--		LBTX[3:0]=0111
		--	2.2	--		LBTX[3:0]=0110
		--	2.1	--		LBTX[3:0]=0101
		--	2.0	--		LBTX[3:0]=0100
Digital I/O parameter						
IOH	Output high current source	--	12	--	mA	VOH=VDD-0.3V，P33
		4.5	--	12	mA	VOH=VDD-0.3V， P27-20
IOL	Output low current sink	--	12	--	mA	VOL=0.3V，P33
		--	72	100	mA	VOL=0.3V，P27-20
VIH	Input high voltage	0.7VDD	--	--	V	--
VIL	Input low voltage	--	--	0.3VDD	V	--
VOH	Output high voltage	VDD-0.3	--	--	V	--
VOL	Output low voltage	--	--	VSS+0.3	V	--
Rpu	Pin pull up resistance	--	5	--	kΩ	VDD = 3.0，P10
		--	50	--		VDD = 3.0，other I/O

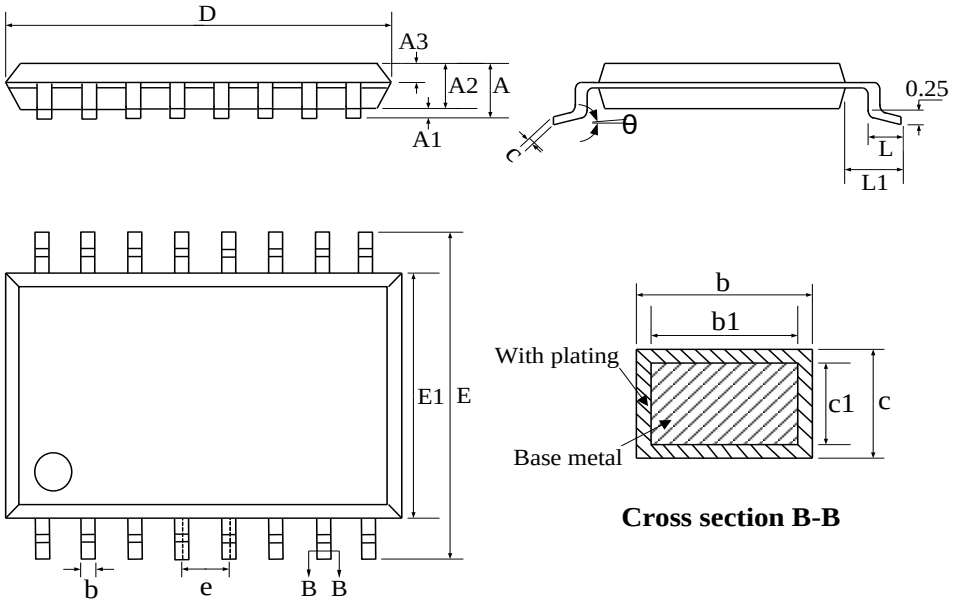
Remarks:

1.Noise free bits and effective resolution are both related to the signal's full scale range. Its peak to peak or rms noise plays the decisive role.

2.The signal input range is limited by the differential signal input range and the absolute voltage at the input terminals. The first one is the real signal input range. It is affected by the PGIA gain and the ADC voltage reference choice. The second one includes both differential and common mode components and is mainly limited by the circuit.

3.Vref is the ADC voltage reference. It originates from AVDDR or AIR and then internally processed, user selectable.

Packaging Information



Dimensions: mm

Symbol	Min.	Nom.	Max.
A	—	—	1.75
A1	0.05	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.48
b1	0.38	0.41	0.43
c	0.21	—	0.26
c1	0.19	0.20	0.21
D	9.70	9.90	10.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
L	0.50	—	0.80
L1	1.05BSC		
θ	0°	—	8°

Figure 8. SOP16 mechanical specification